



28/40/44-Pin Enhanced Flash Microcontrollers

DEVICE OVERVIEW

Devices Included in this Data Sheet:

- PIC16F873A, PIC16F876A, PIC16F874A, PIC16F877A

High-Performance RISC CPU:

- Only 35 single-word instructions to learn
All single-cycle instructions except for program branches, which are two-cycle
Operating speed: DC - 20 MHz clock input
DC - 200 ns instruction cycle
Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM Data Memory
Pinout compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscale
Two Capture, Compare, PWM modules
Synchronous Serial Port (SSP) with SPI (Master mode) and I2C (Master/Slave)
Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
Parallel Slave Port (PSP) - 8 bits wide with external RD, WR and CS controls (40/44-pin only)
Brown-out detection circuitry for Brown-out Reset (BOR)

Analog Features:

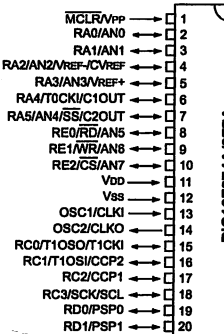
- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
Brown-out Reset (BOR)
Analog Comparator module with:
Two analog comparators
Programmable on-chip voltage reference (VREF) module
Programmable input multiplexing from device inputs and internal voltage reference
Comparator outputs are externally accessible

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced Flash program memory typical
1,000,000 erase/write cycle Data EEPROM memory typical
Data EEPROM Retention > 40 years
Self-reprogrammable under software control
In-Circuit Serial Programming (ICSP) via two pins
Single-supply 5V In-Circuit Serial Programming
Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
Programmable code protection
Power saving Sleep mode
Selectable oscillator options
In-Circuit Debug (ICD) via two pins

Pin Diagrams (Continued)

40-Pin PDIP



This document contains device specific information about the following devices:

- PIC16F873A
PIC16F874A
PIC16F876A
PIC16F877A

PIC16F873A/876A devices are available only in 28-pin packages, while PIC16F874/877A devices are available in 40-pin and 44-pin packages. All devices in the PIC16F877A family share common architecture with the following differences:

- The PIC16F873A and PIC16F874A have one-half of the total on-chip memory of the PIC16F876A and PIC16F877A
The 28-pin devices have three I/O ports, while the 40/44-pin devices have five
The 28-pin devices have fourteen interrupts, while the 40/44-pin devices have fifteen
The 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight
The Parallel Slave Port is implemented only on the 40/44-pin devices

The available features are summarized in Table 1-1. Block diagrams of the PIC16F873A/876A and PIC16F874/877A devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the PIC16C00 Mid-Range Reference Manual (DS00002), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

44-Pin TQFP

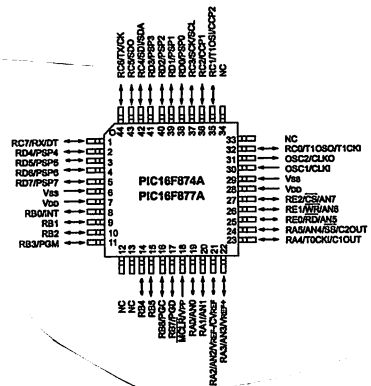


Table with columns: Device, Program Memory (Bytes, # Single Word Instructions), Data SRAM (Bytes), EEPROM (Bytes), I/O, 10-bit A/D (ch), CCP (PWM), MSSP (SPI, Master, I2C), USART, Timers 8/16-bit, Comparators. Rows include PIC16F873A, PIC16F874A, PIC16F876A, and PIC16F877A.

TABLE 1-3: PIC16F744A/77A PINOUT DESCRIPTION

Pin Name	PDP	PLCC	TQFP	QFN	QFP	Buffer Type	Description
OSC1CLKI OSC1	13	14	30	32	1	ST/CMOS ¹⁾	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1CLKI, OSC2CLKI pins).
CLKI					1		
OSC2CLKI OSC2	14	15	31	33	0		Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKI, which has 1/4 the frequency of OSC1 and divides the instruction cycle rate.
CLKO					0		
MCLR/VPP MCLR	1	2	18	18	1	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low Reset to the device. Programming voltage input.
VPP					P		
RA0/AN0 AN0	2	3	19	19	1	TTL	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0.
RA1/AN1 AN1	3	4	20	20	1	TTL	Digital I/O. Analog input 1.
RA2/AN2/VREF-/VREF- AN2	4	5	21	21	1	TTL	Digital I/O. Analog input 2. AD reference voltage (Low) input. Comparator Vref output.
RA3/AN3/VREF+/VREF+ AN3	5	6	22	22	1	TTL	Digital I/O. Analog input 3. AD reference voltage (High) input.
RA4/AN4/SS/C2OUT RA4	6	7	23	23	1	ST	Digital I/O - Open-drain when configured as output. Timer0 external clock input. Comparator 1 output.
RA5/AN5/SS/C2OUT RA5	7	8	24	24	1	TTL	Digital I/O. Analog input 4. SPI slave select input. Comparator 2 output.

Legend: I = input O = output IO = input/output P = power
 -- = Not used TTL = TTL input ST = Schmitt Trigger input
 Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 Note 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
 Note 3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

TABLE 1-3: PIC16F744A/77A PINOUT DESCRIPTION (CONTINUED)

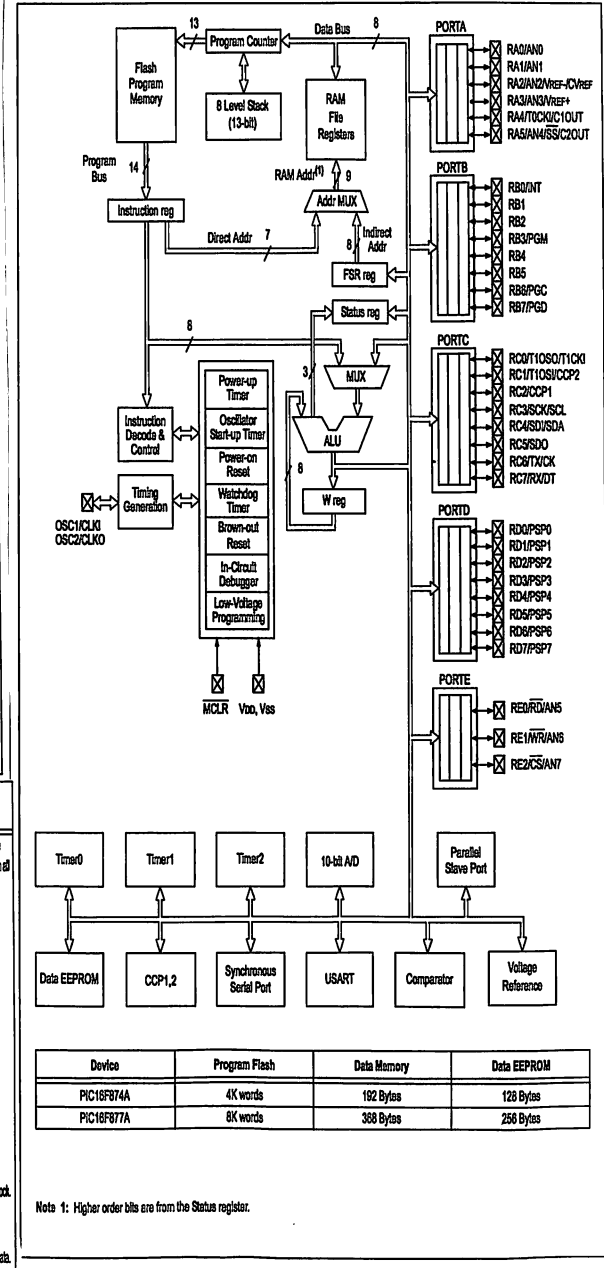
Pin Name	PDP	PLCC	TQFP	QFN	QFP	Buffer Type	Description
RD0/PS0 RD0 PS0	19	21	38	38	1	ST/TTL ²⁾	PORTD is a bidirectional I/O port or Parallel Slave Port when interfacing to a microprocessor bus. Digital I/O. Parallel Slave Port data.
RD1/PS1 RD1 PS1	20	22	39	39	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RD2/PS2 RD2 PS2	21	23	40	40	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RD3/PS3 RD3 PS3	22	24	41	41	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RD4/PS4 RD4 PS4	27	30	2	2	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RD5/PS5 RD5 PS5	28	31	3	3	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RD6/PS6 RD6 PS6	29	32	4	4	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RD7/PS7 RD7 PS7	30	33	5	5	1	ST/TTL ²⁾	Digital I/O. Parallel Slave Port data.
RE0/AN6 RE0 AN6	8	9	25	25	1	ST/TTL ²⁾	PORTE is a bidirectional I/O port. Digital I/O. Reset control for Parallel Slave Port. Analog input 5.
RE1/AN7 RE1 AN7	9	10	26	26	1	ST/TTL ²⁾	Digital I/O. Write control for Parallel Slave Port. Analog input 6.
RE2/AN7 RE2 AN7	10	11	27	27	1	ST/TTL ²⁾	Digital I/O. Chip select control for Parallel Slave Port. Analog input 7.
VSS	12, 31	13, 34	6, 29	6, 30, 31	P		Ground reference for logic and I/O pins.
VDD	11, 32	12, 35	7, 28	7, 8, 28, 29	P		Positive supply for logic and I/O pins.
NC	--	1, 17, 12, 28, 40	13, 33, 34	13	--		These pins are not internally connected. These pins should be left unconnected.

TABLE 1-3: PIC16F744A/77A PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDP	PLCC	TQFP	QFN	QFP	Buffer Type	Description
RC0/T1OS0/T1CKI RC0 T1OS0 T1CKI	15	16	32	34	1	IO	PORTC is a bidirectional I/O port. Digital I/O. Timer1 oscillator output. Timer1 external clock input.
RC1/T1OS1/CCP2 RC1 T1OS1 CCP2	16	18	35	35	1	ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PHM2 output.
RC2/CCP1 RC2 CCP1	17	19	36	36	1	IO	Digital I/O. Capture1 input, Compare1 output, PHM1 output.
RC3/SCK/SCL RC3 SCK SCL	18	20	37	37	1	IO	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode.
RC4/SDA/SDA RC4 SDI SDA	23	25	42	42	1	IO	Digital I/O. SPI data in. I ² C data I/O.
RC5/SDO RC5 SDO	24	26	43	43	1	IO	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	27	44	44	1	IO	Digital I/O. USART asynchronous transmit. USART1 synchronous clock.
RC7/RX/DT RC7 RX DT	26	28	1	1	1	IO	Digital I/O. USART asynchronous receive. USART1 synchronous data.

Pin Name	PDP	PLCC	TQFP	QFN	QFP	Buffer Type	Description
RB0/BT BT	33	36	8	9	1	TTL/ST ³⁾	Digital I/O. External Interrupt.
RB1	34	37	9	10	1	IO	Digital I/O.
RB2	35	38	10	11	1	IO	Digital I/O.
RB3/PGM PGM	36	39	11	12	1	IO	Digital I/O. Low-voltage I ² CSP programming enable pin.
RB4	37	41	14	14	1	IO	Digital I/O.
RB5	38	42	15	15	1	IO	Digital I/O.
RB6/PGC PGC	39	43	16	16	1	TTL/ST ³⁾	Digital I/O. In-circuit debugger and I ² CSP programming clock.
RB7/PGD PGD	40	44	17	17	1	TTL/ST ³⁾	Digital I/O. In-circuit debugger and I ² CSP programming data.

FIGURE 1-2: PIC16F744A/77A BLOCK DIAGRAM



Device	Program Flash	Data Memory	Data EEPROM
PIC16F74A	4K words	192 Bytes	128 Bytes
PIC16F77A	8K words	368 Bytes	256 Bytes

Note 1: Higher order bits are from the Status register.

參考資料